What is claimed is:

ESM00-001

1. A method of forming a composite gate dielectric layer for a thin film transistor (TFT), device, comprising the steps of:

providing an insulating substrate;

providing an active semiconductor layer on said insulating substrate;

thermally growing a first gate dielectric layer, in a furnace, on said active semiconductor layer;

performing a first anneal procedure to change said active semiconductor layer;

thermally depositing a second gate dielectric layer on said first gate dielectric layer; and

performing a second anneal procedure to create a densified second gate dielectric layer, resulting in said composite gate dielectric layer comprised of said densified second gate dielectric on said first gate dielectric layer.

2. The method of claim 1, wherein said active semiconductor layer is a polysilicon layer, obtained via low pressure chemical vapor deposition (LPCVD), procedures, to a thickness between about 500 to 1000 Angstroms.

3. The method of claim 1, wherein said first gate dielectric layer is a silicon oxide layer, at a thickness between about 50 to 150 Angstroms, obtained via thermal oxidation procedures, performed in an ambient comprised of a mixture of oxygen in either argon or nitrogen, at a temperature between about 800 to 1100° C, and performed for a time between about 15 to 30 min.

4. The method of claim 1, wherein said first anneal procedure, used to change said active semiconductor layer, is performed at a temperature between about 900 to 1200° C, in a nitrogen or argon ambient, for a time between about 3 to 5 hrs.

5. The method of claim 1, wherein said second gate dielectric layer is a thermally deposited silicon oxide layer, obtained at a thickness between about 500 to 700 Angstroms, deposited at a temperature between about 600 to 700° C, using tetraethylorthosilicate as a source.

6. The method of claim 1, wherein said second anneal procedure, used to create said densified second gate dielectric layer, is performed at a temperature between about 900 to 1000° C, in an ambient comprised of a mixture of oxygen in either nitrogen or argon.

7. A method of forming a thin film transistor, featuring a composite gate dielectric layer, on an insulating substrate, comprising the steps of:

providing said insulating substrate;

forming a first polysilicon layer on said insulating substrate;

thermally growing a first silicon oxide layer, in a furnace, on said first polysilicon layer;

performing a first anneal procedure, in situ in said furnace, to improve TFT parametric performance;

thermally depositing a second silicon oxide gate dielectric layer, on underlying, said first silicon oxide dielectric layer, via thermal decomposition of tetraethylorthosilicate (TEOS).

performing a second anneal procedure to densify said second silicon oxide gate dielectric layer, resulting in said composite gate dielectric layer, comprised of densified, said second silicon oxide gate dielectric layer on said first silicon oxide gate insulator layer;

depositing a second polysilicon layer;

patterning of said second polysilicon layer, and of said composite gate dielectric layer to create a polysilicon gate structure on said composite gate dielectric layer; and

forming a source/drain region in a portion of said large grain size polysilicon layer, not covered by said polysilicon gate structure.

8. The method of claim 7, wherein wherein said first polysilicon layer is obtained via low pressure chemical vapor deposition (LPCVD), procedures, to a thickness between about 500 to 1500 Angstroms.

9. The method of claim 7, wherein said first silicon oxide gate dielectric layer is thermally grown to a thickness between about 50 to 150 Angstroms, via thermal oxidation procedures performed in an ambient comprised of a mixture of oxygen in either argon or nitrogen, at a temperature between about 800 to 1100° C, and for a time between about 15 to 30 min.

10. The method of claim 7, wherein said first anneal procedure, used to improve TFT parametric performance, is performed at a temperature between about 900 to 1200° C, in a nitrogen or argon ambient, for a time between about 3 to 5 hrs.

11. The method of claim 7, wherein said second silicon oxide gate dielectric layer is a thermally deposited silicon oxide layer, obtained at a thickness between about 500 to 700 Angstroms, deposited at a temperature between about 600 to 700° C, using tetraethylorthosilicate as a source.

12. The method of claim 7, wherein said second anneal procedure, used to densify said second silicon oxide gate dielectric layer, is performed at a temperature between about 900 to 1000° C, in an ambient comprised of a mixture of oxygen, in either nitrogen or argon.

13. The method of claim 7, wherein said second polysilicon layer is obtained via low pressure chemical vapor deposition (LPCVD), procedures, at a thickness between about 3000 to 5000 Angstroms, and either doped in situ, during deposition, via the addition of arsine, or phosphine, to a silane ambient, or doped using PH_3 or $POCl_3$ source in a diffusion tube, or deposited intrinsically then doped via implantation of arsenic or phosphorous ions.

14. The method of claim 7, wherein said polysilicon gate structure, on said composite gate dielectric layer, is formed via a reactive ion etching procedure, using Cl_2 or SF_6 as an etchant for said second polysilicon layer, while using CF_4 or CHF_3 as an etchant for said composite gate dielectric layer.

15. The method of claim 7, wherein said source/drain region is formed via implantation of arsenic or phosphorous ions, at an energy between about 50 to 100 KeV, at a dose between about 1E15 to 1E16 atoms/cm^2.

16. A method of forming a thermally deposited, gate dielectric layer, for a thin film transistor device, comprising the steps of:

providing said insulating substrate;

forming an active semiconductor layer on said insulating substrate;

thermally depositing a silicon oxide gate dielectric layer on said active semiconductor layer, using tetraethylorthosilicate as a source; and

performing an anneal procedure to densify said silicon oxide gate dielectric layer.

17. The method of claim 16, wherein said active semiconductor layer is a polysilicon layer, obtained via low pressure chemical vapor deposition (LPCVD), procedures, to a thickness between about 500 to 1500 Angstroms.

18. The method of claim 16, wherein said silicon oxide gate dielectric layer is a thermally deposited silicon oxide layer, obtained at a thickness between about 500 to 700 Angstroms, deposited at a temperature between about 600 to 700° C, using tetraethylorthosilicate as a source.

19. The method of claim 16, wherein said anneal procedure, used to densify said silicon oxide gate dielectric layer, is performed at a temperature between about 900 to 1000° C, in an ambient comprised of a mixture of oxygen in either nitrogen or argon.